Tytuł:

Szybkie układy scalone do precyzyjnego pomiaru czasu w strukturach pikselowych w technologiach nanometrycznych (2018 – 2023)

Title:

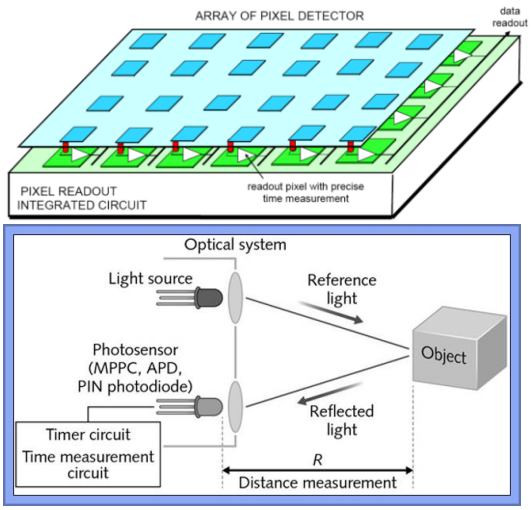
Fast integrated circuits for precise time measurements in pixel structures in nanometers technologies (2018 – 2023)

Principal Investigator:

Prof. dr inż. Bogdan Staszewski

Financing Institution:

National Science Centre, Poland, under Contract No. UMO-2017/27/B/ST7/01217



The hybrid detector, its potential application and hypothetical time based measurement idea.

The aim of this project was the exploration and realization of a new concept of massively parallel time-to-digital converters (TDC) that are realized in a nanometer-scale CMOS process technology and are optimized for time-of-flight (ToF)-based matrix of pixel detectors. The TDCs are used to digitize the detected time-of-arrival of a photon (e.g., X-ray, infrared) or a particle, while denoting the detector's position within the matrix (i.e., spatiotemporal detection). Given a large number (thousands or even millions in the future) of intended pixels to be supported, each pixel detector is envisioned to be served by a dedicated TDC. This will maximally increase the detection speed/rate while keeping its detection unavailability (i.e., "dead time") to a minimum. The key TDC parameters are: fine picosecond-level resolution, small area and low power consumption; hence, they are best implemented in nanometer-scale (nanoscale) CMOS process technology. Unfortunately, this process choice makes it incompatible with the photon/particle detectors, whose key parameters are the quantum and detection efficiencies in the intended spectrum range, which rarely agrees with that of silicon. The hybrid detector thus attempts to solve this technology mismatch problem by stacking the pixel detector

die on top of the CMOS silicon die of TDC matrix, while interconnecting them with tiny bump bondings. In this arrangement, the TDC dimensions must naturally be lower than the pitch of pixel detectors, which is now typically around 50-100 μm but expected to continue shrinking in the future. Time-of-flight (ToF) measurements are becoming essential to the advancement of detectors for positron emission tomography (PET), high-energy physics, 3D vision, ultra-high-resolution microscopy, near-infrared imaging, tie resolved Raman spectroscopy, quantum security, and many others. In many of these applications, a real-time millimeter-level timing resolution along the direct line of response is required. During the realization of the project Authors managed to design, send to fabrication, and perform measurements few integrated circuits including two with multichannel pixel architecture chip. The pixel shaped chip versions are developed to be able to connect with pixel shaped detector and in that way allow building the hybrid detector (the one composed of two independent modules, i.e. integrated circuit and detector that are combined with bump bonding technique). Additionally, project Authors intensively worked on individual integrated blocks that are a part of the final time to digital system, i.e. two different new PLLs architectures for precise signal clock generation were proposed, modern band pass filters and low noise amplifiers were developed, and two ADCs architectures were designed and tested. Importantly, great part of the work was devoted to propose new techniques for mitigating the process, voltage, and temperature negative effects on the working circuits. These are circuits that work automatically and in parallel to main blocks and monitor any disturbances from supply lines, or the process and temperature influence and provide feedback compensation signal. These methods were also verified by extensive measurements and proved their efficiency. The new solutions and methods worked out during this project will have a great deal of universal value and applicability, so they are expected to be used in other applications, especially where it is important to swiftly process precise timing signals while maintaining low power consumption.

Journal / Conference Papers:

1. *Increasing the Position Resolution in Single Photon Counting Pixel Readout IC by Real-Time Interpixel Communications*, P. Otfinowski, D. Magalhães, P. Fajardo, P. Grybos, R. Kleczek, P. Kmon, and M. Ruat, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, submitted for publication in January 2024.
2. *SPHIRD–Single Photon Counting Pixel Readout ASIC With Pulse Pile-Up Compensation Methods*, P. Grybos, R. Kleczek, P. Kmon, P. Otfinowski, P. Fajardo, D. Magalhães, and M. Ruat, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, 2023, 10.1109/TCSII.2023.3267859.
3. *Single Photon Counting Readout IC With 44 e− rms ENC and 5.5 e− rms Offset Spread With Charge Sensitive Amplifier Active Feedback Discharge*, R. Kleczek, P. Kmon, P. Maj, R. Szczygiel, M. Zoladz, and P. Grybos, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, 2023, 10.1109/TCSI.2023.3241738.
4. *Small pixel high-spatial resolution photon-counting prototype IC for synchrotron applications*, P. Grybos, R. Kleczek, P. Kmon, P. Otfinowski, and P. Fajardo, Journal of Instrumentation, Vol. 18, 2023, 10.1088/1748-0221/18/01/C01052.
5. *Multichannel integrated circuit for time-based measurements in 28 nm CMOS*, L.A. Kadlubowski, P. Kmon, Journal of Instrumentation, Volume 19, 2024, 10.1088/1748-0221/19/02/C02004.
6. *Recording channel design for time-based measurements in 28nm CMOS*, L.A. Kadlubowski, P. Kmon, Journal of Instrumentation, Volume 18, 2023, 10.1088/1748-0221/18/10/P10028.
7. *Design, Verification and Testing of a Readout Integrated Circuit for Hybrid Pixel X-ray Detectors with in-Pixel Time Measurement Functionality in 28 nm CMOS*, L. A. Kadlubowski, Mixed Design of Integrated Circuits and Systems – MIXDES 2023, 10.23919/MIXDES58562.2023.10203236.
8. *A 529-μW Fractional-N All-Digital PLL Using TDC Gain Auto-Calibration and an Inverse-Class-F DCO in 65-nm CMOS*, Peng Chen, Xi Meng, Jun Yin, Pui-In Mak, Rui P. Martins, and Robert Bogdan Staszewski, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, 2022, 10.1109/TCSI.2021.3094094.
9. *A Fractional-N Digitally Intensive PLL Achieving 428-fs Jitter and <−54-dBc Spurs Under 50-mVpp Supply Ripple*, Yue Chen, Jiang Gong, Robert Bogdan Staszewski, and Masoud Babaie, IEEE JOURNAL OF SOLID-STATE CIRCUITS, 2022, 10.1109/JSSC.2021.3123386.
10. *Mismatch Analysis of DTCs With an Improved BIST-TDC in 28-nm CMOS*, Peng Chen, Jun Yin, Feifei Zhang, Pui-In Mak, Rui P. Martins, and Robert Bogdan Staszewski, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, 2022, 10.1109/TCSI.2021.3105451.
11. *A Clock-Phase Reuse Technique for Discrete-Time Bandpass Filters*, Amir Bozorg, and Robert Bogdan Staszewski, IEEE JOURNAL OF SOLID-STATE CIRCUITS, 2022, 10.1109/JSSC.2021.3086621.
12. *Design of Prototype Readout Integrated Circuit for Time-of- Arrival and Time-over-Threshold Measurement for Hybrid Pixel X-ray Detectors in 28 nm CMOS*, Lukasz A. KADLUBOWSKI, Piotr KMON, Przegląd Elektrotechniczny, 2022, 10.15199/48.2022.02.23.
13. *Pomiar krótkich odcinków czasu z wykorzystaniem przetwornika czas-cyfra w architekturze Verniera z oscylatorami pierścieniowymi w technologii CMOS 28 nm*, Łukasz A. KADŁUBOWSKI, Piotr KMON, Przegląd Elektrotechniczny, 2020, 10.15199/48.2020.12.22.
14. *Interchannel Mismatch Calibration Techniques for Time- Interleaved SAR ADCs*, MOJTABA BAGHERI, FILIPPO SCHEMBARI, HASHEM ZAREHOSEINI, ROBERT BOGDAN STASZEWSKI, AND AROKIA NATHAN, IEEE Open Journal of Circuits and Systems, 2021, 10.1109/OJCAS.2021.3083680.
15. *A 38.6-fJ/Conv.-Step Inverter-Based Continuous-Time Bandpass ADC in 28 nm Using Asynchronous SAR Quantizer*, Hanie Ghaedrahmati, Jianjun Zhou, and Robert Bogdan Staszewski,

IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, 2021, 10.1109/TCSII.2021.3089831.

16. *An 85-GHz Low-Power Low-Noise Amplifier with 15 GHz Bandwidth in 22nm FD-SOI CMOS for 5G Communications*, Amir Bozorg, Slawomir Gruszczynski, and Bogdan Staszewski, MIKON 2022, 10.23919/MIKON54314.2022.9924886.
17. *Pomiar krótkich odcinków czasu z wykorzystaniem przetwornika czas-cyfra w architekturze Verniera z oscylatorami pierścieniowymi w technologii CMOS 28 nm*, Łukasz A. KADŁUBOWSKI, Piotr KMON, Krajowa Konferencja Elektroniki, 2020.
18. *Digital Controller for Multichannel Time to Digital Converter in 28nm CMOS Process*, G. Wegrzyn , P. Kmon, B. Staszewski, Engineering in Medicine & Biology Society International Student Conference 2020.
19. *SPC Pixel IC with 9.4 e− rms Offset Spread, 60 e− rms ENC and 70 kfps Frame Rate*, 49th European Solid-State Device Research Conference and 45th European Solid-State Circuits Conference, 2019.
20. *Test and Verification Environment and Methodology for Vernier Time-to-Digital Converter Pixel Array*, Lukasz A. Kadlubowski, Piotr Kmon, 2021 24th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), 2021, 0.1109/DDECS52668.2021.9417054.
21. *Design of Prototype Readout Integrated Circuit for Time-of- Arrival and Time-over-Threshold Measurement for Hybrid Pixel X-ray Detectors in 28 nm CMOS*, Lukasz A. KADLUBOWSKI, Piotr KMON, 10.15199/48.2016, Krajowa Konferencja Elektroniki, 2021.

Presented research results:

1. 49th European Solid-State Device Research Conference and 45th European Solid-State Circuits Conference, 2019.
2. MIKON, 24th international Microwave and Radar Conference, 2022.
3. Engineering in Medicine & Biology Society International Student Conference 2020
4. 24th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), 2021.
5. 24th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), 2021.
6. Krajowa Konferencja Elektroniki, 2020.
7. Krajowa Konferencja Elektroniki, 2021.